WHAT IS CLAIMED IS:

1. A shift register circuit comprising:

a first shift register having a plurality of stages connected in cascade; and

a second shift register having more stages than the first shift register;

wherein the stages of the second shift register are divided into groups each formed of consecutive stages, and

the stages of the first shift register are configured to transmit output pulse sequences having a predetermined number of consecutive pulses and having different phases from each other, to the stages constituting the groups of the second shift register as clock signals.

2. A shift register circuit according to Claim 1, wherein the first shift register has an input terminal configured to receive a pulse sequence having a finite number of consecutive pulses.

3. A shift register circuit according to Claim 1, wherein the first shift register is a bi-directional shift register.

4. A shift register circuit according to Claim 2, wherein a plurality of the second shift registers is provided.

5. A shift register circuit according to Claim 1, further comprising an active matrix circuit having switching devices associated with intersections of signal lines and scanning lines, the scanning lines configured to receive outputs of the stages of the second shift register as scanning signals.

6. A shift register circuit according to Claim 5, the active matrix circuit and the second shift register comprising MIS transistors of the same type.

7. A shift register circuit according to Claim 5, the active matrix circuit and the second shift register comprising MIS transistors fabricated from one of amorphous silicon and polycrystalline silicon.

8. A shift register circuit according to Claim 5, further comprising a substrate on which the second shift register and the active matrix circuit are disposed.

9. A shift register circuit according to Claim 2,

wherein each stage of the second shift register has as terminals only:

clock input terminals configured to receive n-phase (n is an integer of at least two) clock signals;

an input terminal configured to receive a signal

sent one of from an input terminal of the second shift register and from an output terminal of a previous stage; and

an output terminal configured to output a signal to one of to an input terminal of a subsequent stage and to an output terminal of the second shift register, and

an initial-stage level configured to initialize a state of each stage of the second shift register input to a selected stage at one of the clock input terminals.

10. A display apparatus comprising a shift register circuit according to Claim 1.

11. A display apparatus according to Claim 10, further comprising an active matrix circuit having switching devices associated with intersections of signal lines and scanning lines, the scanning lines configured to receive outputs of the stages of the second shift register as scanning signals.

12. A display apparatus according to Claim 11, the active matrix circuit and the second shift register comprising MIS transistors of the same type.

13. A display apparatus according to Claim 11, the active matrix circuit and the second shift register comprising MIS transistors fabricated from one of amorphous silicon and polycrystalline silicon.

14. A display apparatus according to Claim 11, further comprising a substrate on which the second shift register and the active matrix circuit are disposed.

15. An image sensor comprising a shift register circuit according to Claim 1.

16. An image sensor according to Claim 15, further comprising an active matrix circuit having switching devices associated with intersections of signal lines and scanning lines, the scanning lines configured to receive outputs of the stages of the second shift register as scanning signals.

17. An image sensor according to Claim 16, the active matrix circuit and the second shift register comprising MIS transistors of the same type.

18. An image sensor according to Claim 16, the active matrix circuit and the second shift register comprising MIS transistors fabricated from one of amorphous silicon and polycrystalline silicon.

19. An image sensor according to Claim 16, further comprising a substrate on which the second shift register and the active matrix circuit are disposed.

20. A shift register circuit according to Claim 1, each group of the second shift register configured to receive output pulses from a set of the stages of the first shift register, the output pulses from the set of stages supplied to each group being isolated from every other group.

21. A shift register circuit according to Claim 1, the stages in each group of the second shift register being divided into an even group configured to receive an even field of output pulses supplied to stages in the even group and an odd group configured to receive an odd field of output pulses supplied to stages in the odd group, the even and odd fields of each group having different timings of the output pulses.

22. A shift register circuit according to Claim 21, the even and odd groups each configured to receive a single start pulse with different timings.

23. A shift register circuit according to Claim 1, each group having at least at many stages as clock signals, each stage in each group having input terminals configured to receive the same number of clock signals, at least one stage in a particular group having the clock signals supplied in a different order from at least one other stages in the particular group.

24. A shift register circuit according to Claim 1, excluding an initial and final stage, the stages having input terminals configured to receive an output from an immediately previous stage and an output from an immediately subsequent stage.

25. A shift register circuit comprising:

at least one second shift register having a plurality of stages connected in cascade, the at least one second shift register divided into groups of consecutive stages; and

clock lines connected with the stages in each group, the clock lines configured to supply clock signals to the stages, the clock lines of each group isolated from the clock lines in each other group, the clock signals having a predetermined number of consecutive pulses with different phases from each other.

26. A shift register circuit according to Claim 25, each stage comprising terminals, the terminals including:

clock input terminals configured to receive the clock signals;

a first input terminal configured to receive an output signal from one of an output terminal of a previous stage and an external start pulse; and

an output terminal configured to receive an output signal.

27. A shift register circuit according to Claim 26, the terminals further comprising a second input terminal configured to receive an output signal from an output terminal of a subsequent stage.

28. A shift register circuit according to Claim 27, wherein the second input terminal is configured to receive an output signal from an immediately previous stage and an output signal from an immediately subsequent stage.

29. A shift register circuit according to Claim 25, further comprising a first shift register having fewer stages than the second shift register, the stages of the first shift register configured to supply the clock signals to the clock lines.

30. A shift register circuit according to Claim 25, the stages in each group of the second shift register being divided into an even group configured to receive an even field of output pulses supplied to stages in the even group and an odd group configured to receive an odd field of output pulses supplied to stages in the odd group, the even and odd fields of each group having different timings of the output pulses, the even and odd groups each having a single start pulse with different timings.

31. A shift register circuit according to Claim 25, each group having at least at many stages as clock signals, each stage in each group having input terminals configured to receive the same number of clock signals, at least one stage in a particular group configured to receive the clock signals supplied differently from at least one other stage in the particular group.

32. A method of increasing reliability of a shift register circuit having a first and second shift register, the method comprising:

dividing stages in the second shift register into groups of consecutive stages;

supplying clock lines of the second shift register with clock signals of different phases from the first shift register; and

isolating the clock lines between groups.

33. A method according to Claim 32, further comprising reducing a wiring resistance and capacitance of the clock lines by reducing a length and a line width of the clock lines.

34. A method according to Claim 32, further comprising reducing at least one of a number and duration of pulses applied to the first shift register and second shift register.

35. A method according to Claim 32, further comprising forming the clock lines on a thin film transistor substrate and forming TCP wiring connecting the clock lines with the first shift register.

36. A method according to Claim 32, further comprising receiving an output signal from a previous stage in a particular stage and supplying an output signal to a subsequent stage from the particular stage.

37. A method according to Claim 36, further comprising feeding back an output signal from the subsequent stage in the particular stage.

38. A method according to Claim 32, further comprising supplying pulses through stages in the first shift register, decreasing a number of the pulses used effectively and supplied to the clock lines.

39 A method according to Claim 32, further comprising dividing the groups into even group having an even field of output pulses supplied to stages in the even group and an odd group having an odd field of output pulses supplied to stages in the odd group, initiating the even and odd groups with a single start pulse, and differing timings of the output pulses between the even and odd fields of each group.

40. A method according to Claim 32, further comprising supplying the same clock signals to all stages in a particular group and supplying the clock signals to at least one of the stages in the particular group differently from at least one other stage in the particular group.

41. A method according to Claim 32, further comprising fixing the clock signals from all stages of the first shift register to a low level after clock pulses pass through each stage of the first shift register.